

Patterned SOI Regions on Semiconductor Chips

Abstract Of The Invention

A method and structure for forming patterned SOI regions and bulk regions is described wherein a silicon containing layer over an insulator may have a plurality of selected thickness' and wherein bulk regions may be suitable to form DRAM's and SOI regions may be suitable to form merged logic such as CMOS. Ion implantation of oxygen is used to formed patterned buried oxide layers at selected depths and mask edges may be shaped to form stepped oxide regions from one depth to another. Trenches may be formed through buried oxide end regions to remove high concentrations of dislocations in single crystal silicon containing substrates. The invention overcomes the problem of forming DRAM with a storage capacitor formed with a deep trench in bulk Si while forming merged logic regions on SOI.